patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

REMARKS

In response to the Office Action dated 5 July 2000, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 21-33 and 36-75 are pending in the application, and are rejected. Claims 22, 25, 27, and 28 have been cancelled, and claims 21, 23, 24, 26, 32, 43, 45, 50, 52, 55, 57, 60, 62, 65, 67, 68, 70, 73, and 75 have been amended to obviate the rejections under 35 USC § 112 only. No new matter has been added. None of the claims were amended to overcome the rejections based on cited references.

Rejections Under 35 USC § 112

Claims 43-75 were rejected under 35 USC § 112, first paragraph. Claims 43, 50, 55, 60, 65, 68, and 73 have been amended to include "wherein x is between 0 and 1.0" to obviate the rejection.

Claims 22, 25, 27, 32, 45, 52, 57 and 60-75 were rejected under 35 USC § 112, second paragraph. Claims 22, 25, and 27 have been cancelled and claims 32, 45, 52, 57, 62, and 67 have been amended to obviate the rejection.

The Examiner rejected claims 60-75 based on the similarity of the limitations recited in claims 60-64 and 68-72, and the similarity of the limitations recited in claims 65-67 and 73-75. MPEP 706.03(k) states that "..court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough." The applicant respectfully submits that a

memory cell may or may not include a transistor, and that a transistor may or may not be a memory cell. Therefore, claims 60-64 and 68-72 have different scope, and claims 65-67 and 73-75 have different scope. The applicant respectfully submits that these claims satisfy the requirements of 35 USC § 112, and are in condition for allowance.

Rejection Under 35 USC § 102

Claims 21-33 and 36-75 were rejected under 35 USC § 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Forbes et al. (U.S. Patent No. 5,886,368, Forbes). The applicant respectfully traverses.

The above-identified application, Serial No. 09/256,643, is a division of the applicants' prior U.S. application, Serial No. 08/903,452, filed on July 29, 1997, which is relied upon for an earlier filing date under 35 U.S.C. §120. The filing date of July 29, 1997 is confirmed by a corrected filing receipt in that application mailed on 6 July 2000 for 08/903,452. Forbes has the same filing date of July 29, 1997. Therefore, Forbes is not prior art.

Rejection Under 35 USC § 103

Claims 21-33 and 36-75 were rejected under 35 USC § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,449,941, Yamazaki) in view of Halvis et al. (U.S. Patent No. 5,369,040, Halvis). The applicant respectfully traverses.

Claim 21 recites a method of fabricating a transistor in a semiconductor substrate including, among other elements, forming a source region and a drain region, a channel region being between the source region and the drain region, forming an insulating layer on the channel region, forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$, and selecting x to be between 0 and 1.0.

Yamazaki is deficient in the following respects. Yamazaki discloses in Figures 2A-2D steps for forming a memory cell with a source region 203, a drain region 204, an oxide film 205, a floating gate 208, and a control gate 210. However, as the Examiner stated, Yamazaki does not disclose forming a gate on an insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$, as recited in claim 21.

Halvis discloses a MOS photodetector with closely-spaced gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon. However, Halvis does not disclose forming a source region and a drain region, a channel region being between the source region and the drain region, and forming an insulating layer on the channel region as recited in claim 21.

The Examiner stated that it would have been obvious to one of ordinary skill in the art to replace the gate of Yamazaki with the gate disclosed by Halvis. The applicant respectfully traverses. There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

There is no teaching in either Yamazaki or Halvis for the combination put forward by the Examiner. Yamazaki discloses a memory cell with a source region 203, a drain region 204, a floating gate 208, and a control gate 210. Halvis discloses a MOS photodetector with multiple gates but no source or drain. The structures are very different and operate in a different manner, so one skilled in the art would not find a teaching in either for the combination. Furthermore, Yamazaki teaches away from the combination. The invention of Yamazaki includes a thin insulator 105 of silicon carbide formed selectively on a part of the drain 104 shown in Figures 1B to 1D. Column 4, lines 7-14 and 27-29 and column 6, lines 1-9. The silicon carbide insulator 105 is directly between the drain 104 and the floating gate 107. Therefore, one skilled in the art would not have been motivated to form either the floating gate 107 or the control gate 109 shown in Figure 1D from the same material as the insulator 105.

The applicant respectfully submits that claim 21 is not disclosed or suggested by the combination of Yamazaki and Halvis, and that claim 21 is in condition for allowance. Claims 22-33 and 36-42 are dependent on claim 21, and recite further limitations with respect to claim 21. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 22-33 and 36-42 are not disclosed or suggested by the combination of Yamazaki and Halvis, and that claims 22-33 and 36-42 are in condition for allowance.

Claims 43-75 recite limitations similar to those recited in claim 21. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 43-75 are not disclosed or suggested by the combination of Yamazaki and Halvis, and that claims 43-75 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5 OCT 2000 By _____

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents, Washington, D.C. 20231 on **October 5, 2000**.

Tina Pugh
Name

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Signature